REMARKS

Claims 1-22 have been examined, with claims 1-3, 8-18, and 22 rejected, and claims 4-7 and 19-21 objected to.

Applicant thanks the Examiner for the indication of allowable subject matter in claims 4-7 and 19-21.

Claims 19 and 21 and the specification have been amended to correct minor informalities.

Claims 1-3, 8-18, and 22 have been rejected under 35 USC 102(b) as being anticipated by Janik et al. (U.S. Patent No. 6,754,116; hereinafter, "Janik"). Applicant respectfully traverses this rejection for the reasons set forth below.

Independent claim 1 is directed to a microprocessor system having an address generator (212) configured to simultaneously generate a first memory address and a second memory address; a memory system (220) having a first memory tower (T0-T3) and a second memory tower (T0-T3); and an address selector (213) coupled to receive the first memory address and the second memory address and configured to select a first row address for the first memory tower and a second row address for the second memory tower. (See Fig. 2.) Independent claim 17 is a method claim corresponding to claim 1.

Janik, which Applicant notes is assigned to the same assignee as the present application, Infineon Technologies AG, is directed to a semiconductor circuit 1 having a processor 3, which converts single-bank commands I generated by BIST processor 2 into multibank commands II. The multibank commands II can be executed by a plurality of memory banks A, B simultaneously. (See Fig. 2.)

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Janik does not teach an address generator configured to simultaneously *generate* a first memory address and a second memory address, as required by the claimed invention. Although Janik simultaneously *executes* the multibank commands II (col. 8, lines 5-6; col. 9, lines 4-8) by accessing memory banks A and B simultaneously, the BIST processor 2 *generates* the single bank commands I *serially* (col. 8, lines 18-21 and 56-58; col. 9, lines 1-2). Thus, the independent claims are patentable over Janik for at least this reason.

Additionally, Janik does not teach a memory system having a first memory tower and a second memory tower, as also required by the claimed invention. Rather, Janik teaches two memory banks A and B. Thus, the independent claims are patentable over Janik for this additional reason.

Claims 2, 3, and 8-16 depend from claim 1, and claims 18 and 22 depend from claim 12. Applicant submits that these dependent claims are patentable for at least the same reasons as discussed above with respect to their respective base claims. Applicant therefore respectfully requests reconsideration and withdrawal of the prior art rejection.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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